

Fig. 1

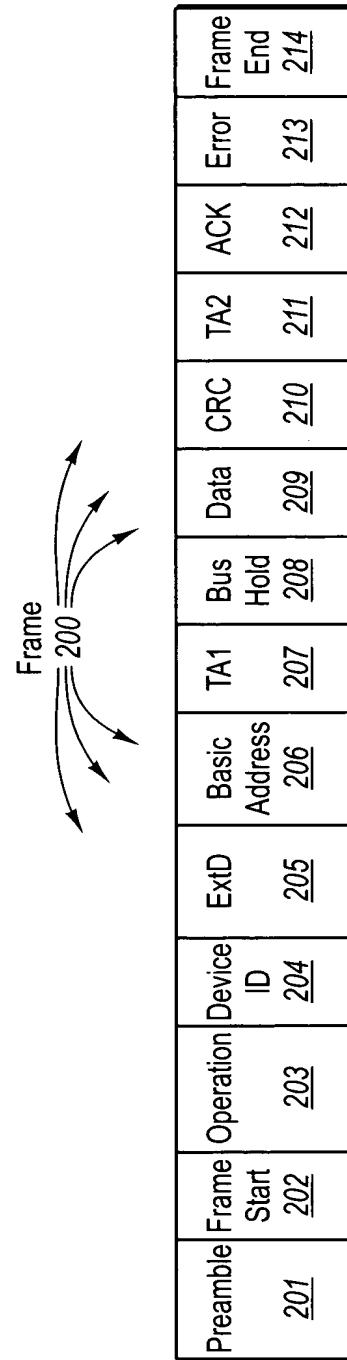


Fig. 2

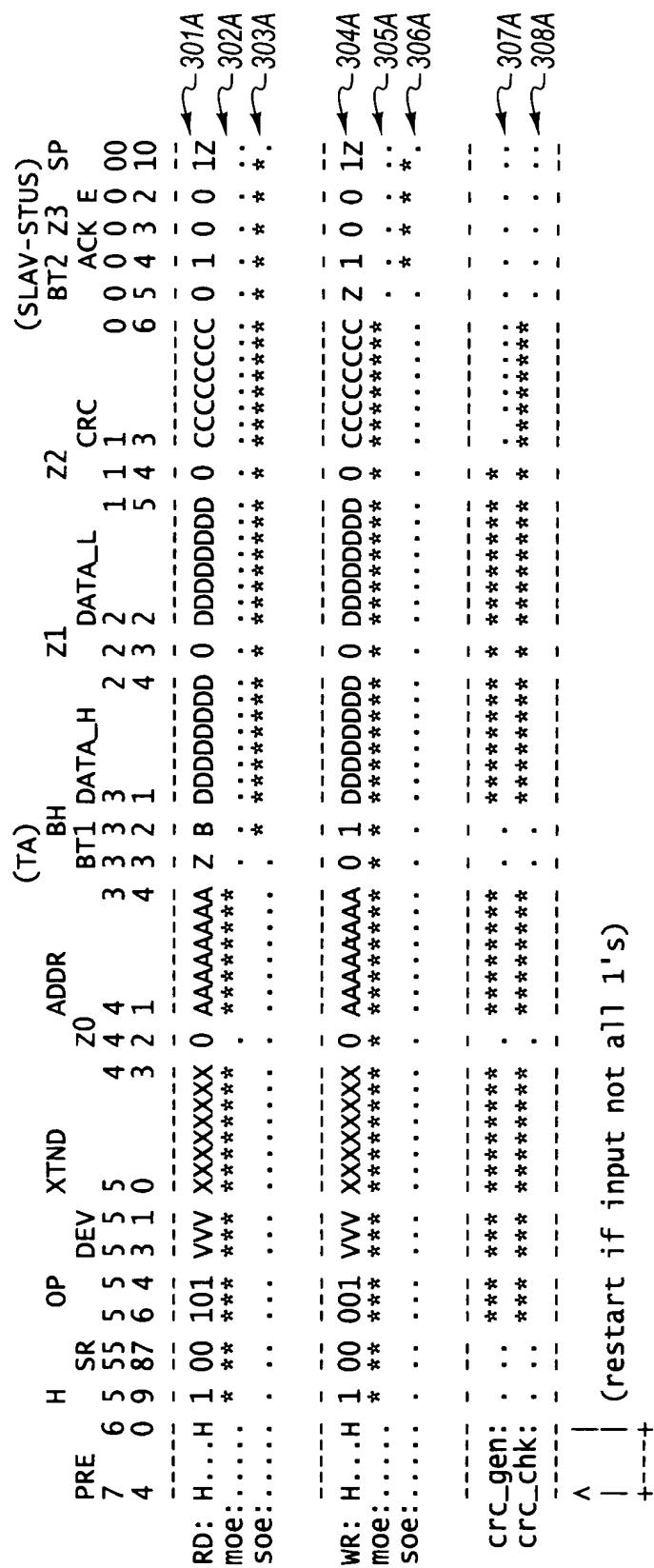


Fig. 3A

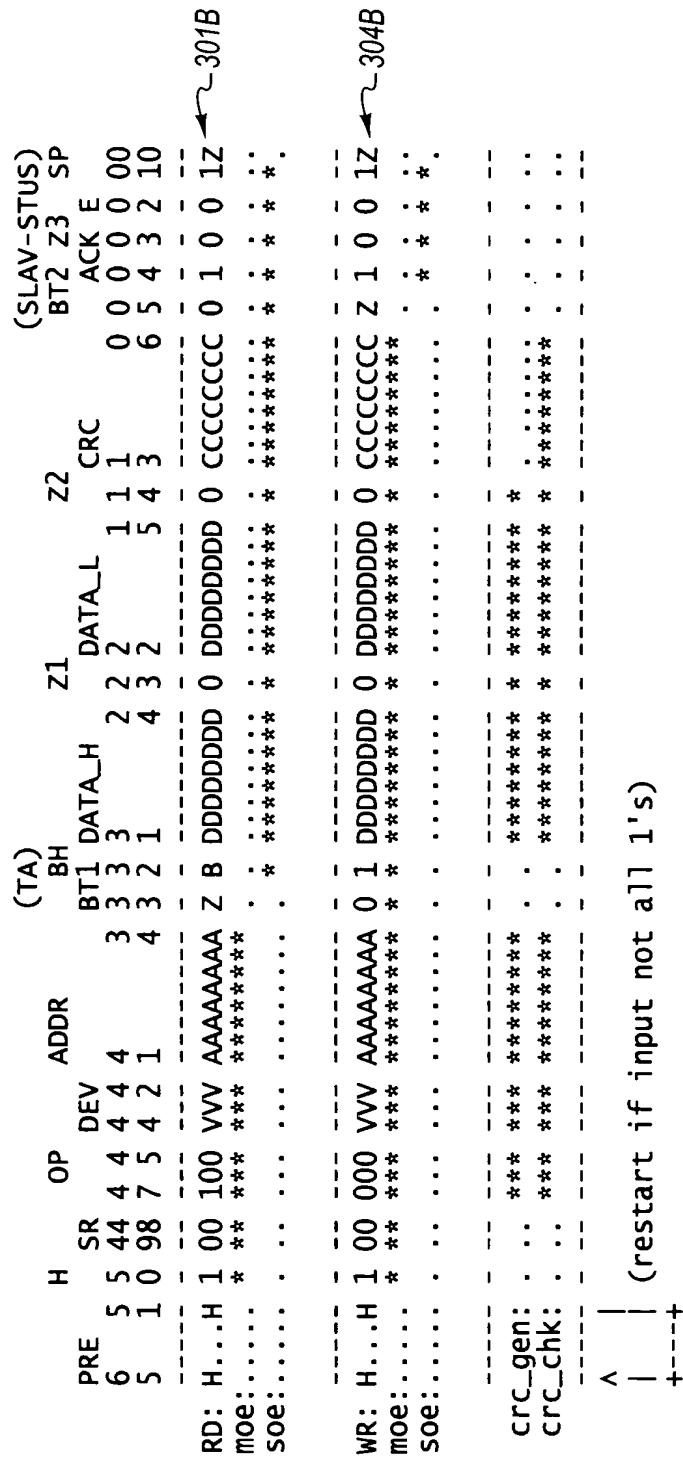


Fig. 3B

Title: TWO-WIRE INTERFACE HAVING EMBEDDED PER

FRAME RELIABILITY INFORMATION

Inventors: Gerald L. Dybsetter and Jayne C. Hahn

Docket No.: 15436.367.1

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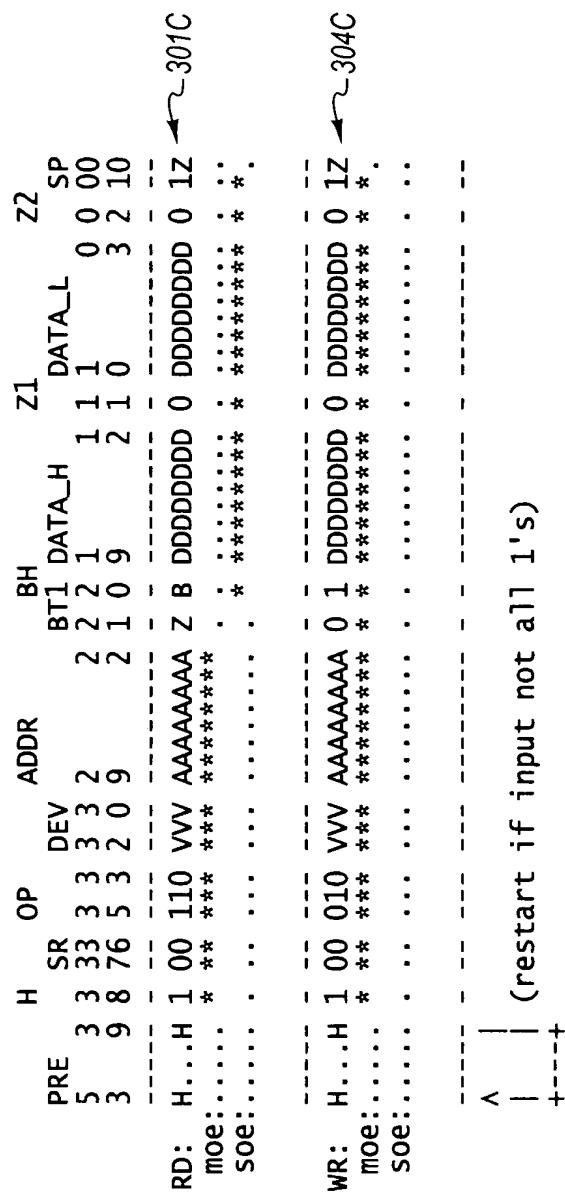


Fig. 3C

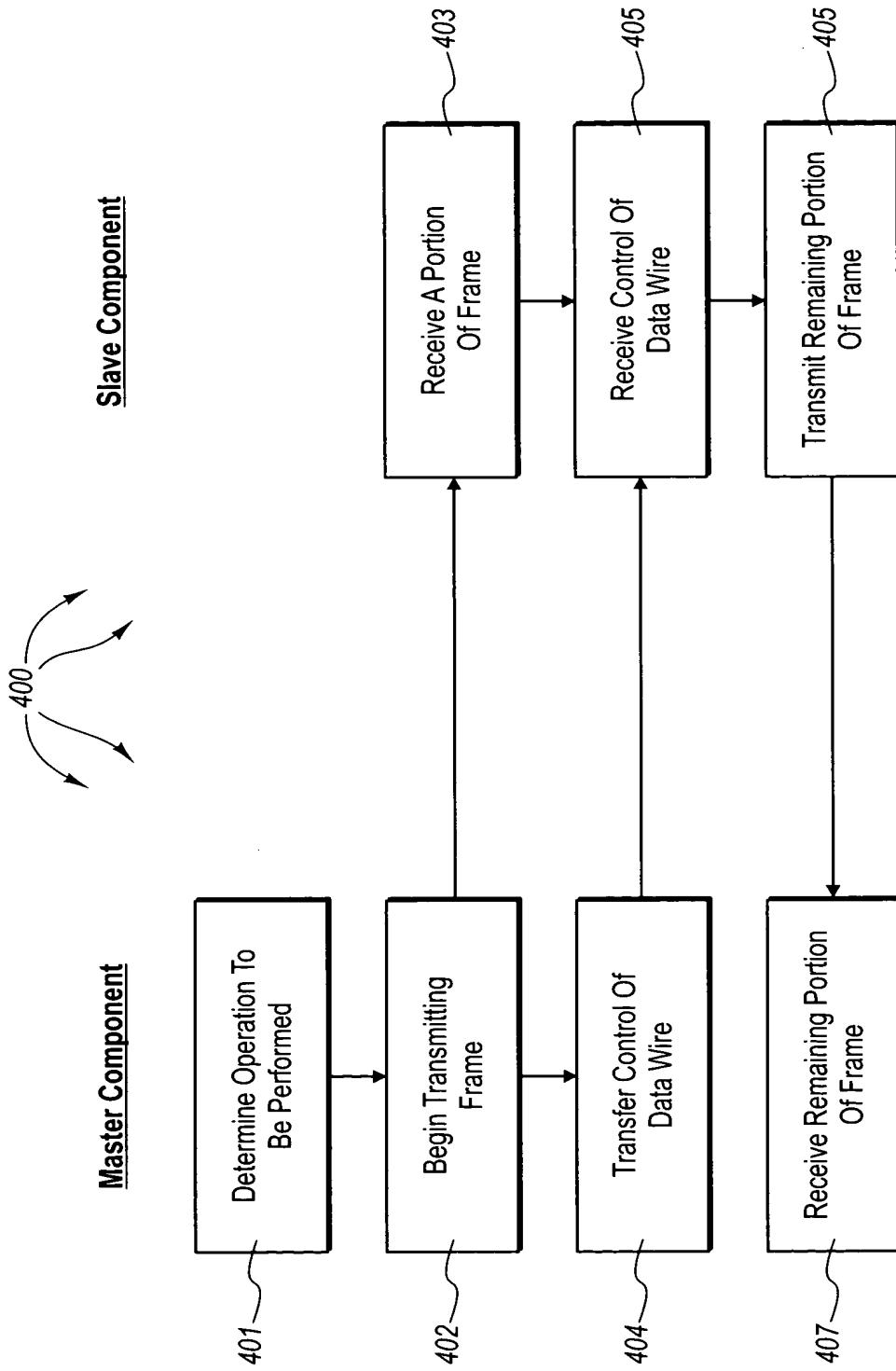


Fig. 4

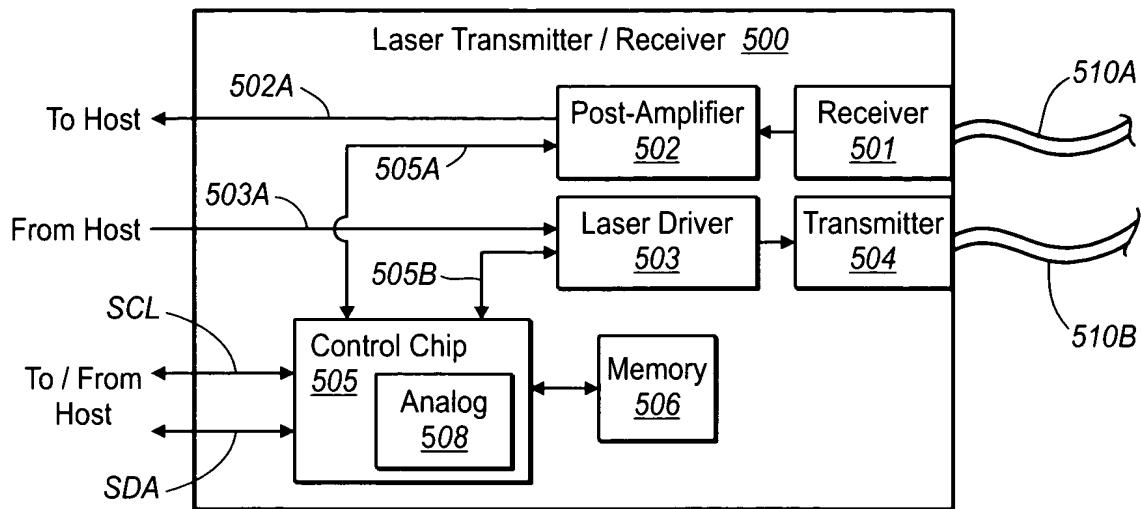


Fig. 5

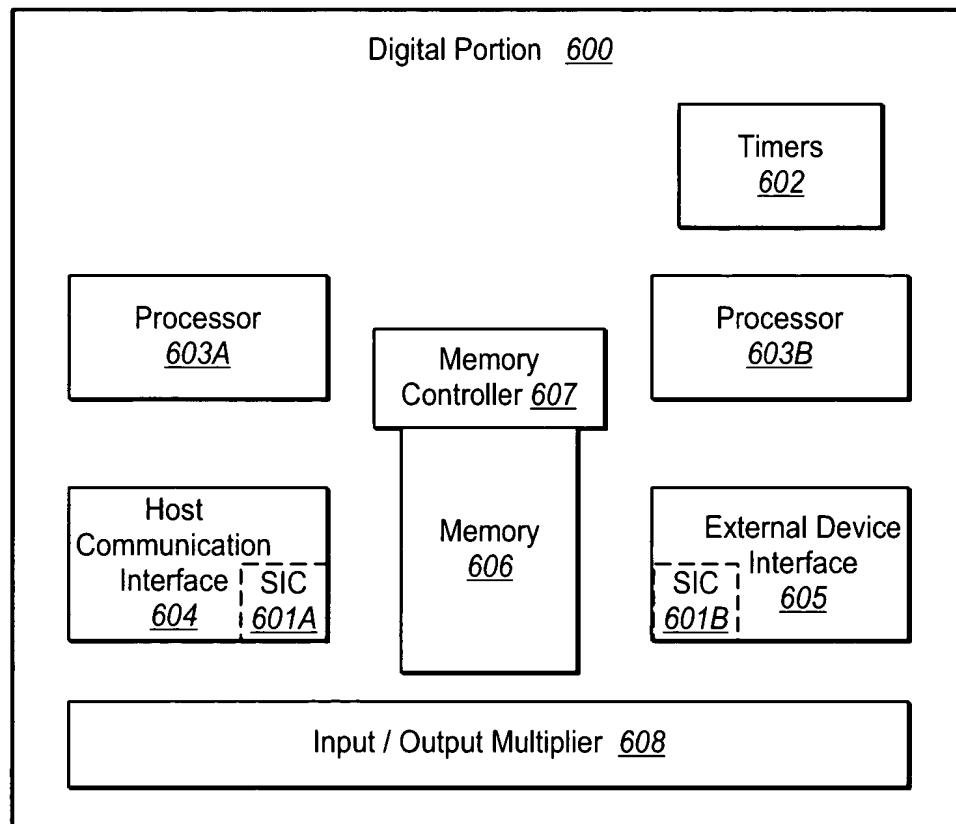


Fig. 6

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	PRE	ST	OP	PRT	DEV	TA	ADDRESS/DATA	IDLE
	6	3	33	32	2	2	1	11 1 0 0
		4	3	21	09	8	4	3 9 87 6 1 0
Address	1...1	00	00	PPPPP	EEEE	10	AAAAA	AAAAA Z
Write	1...1	00	01	PPPPP	EEEE	10	DDDDDDDDDDDDDD	Z
Read	1...1	00	11	PPPPP	EEEE	20	DDDDDDDDDDDDDD	Z
Read inc.	1...1	00	10	PPPPP	EEEE	20	DDDDDDDDDDDDDD	Z

Field	Bits	
PRE	64:33	(32) -- preamble
ST	32:31	(2) -- start of frame
OP	30:29	(2) -- operation code
(ADDR=00, WR=01, RD=11, RDINC=10)		
PRTAD	28:26	(5) -- port address
DEVAD	25:19	(5) -- device address
TA	18:17	(2) -- bus turnaround phase & transfer acknowledge
ADDR/DATA	16:1	(16) -- address or data
IDLE	0	(1) -- end of transmission
	65	-- transaction bit length

Fig. 7
(Prior Art)